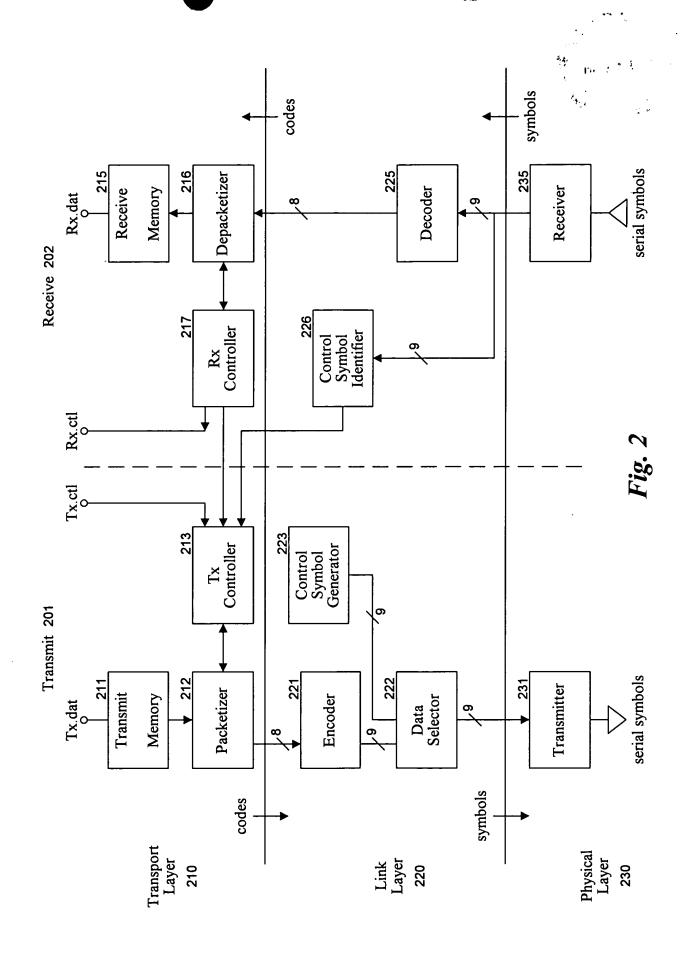
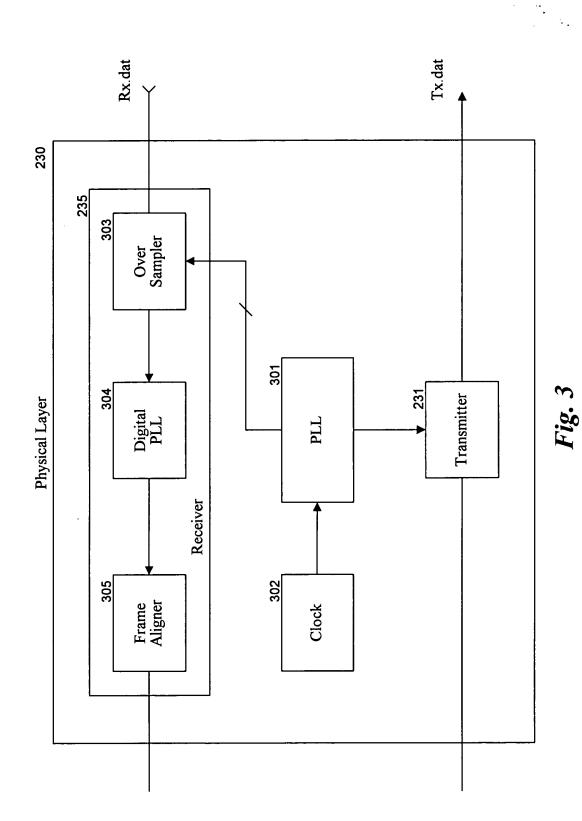


Fig. 1

AS AS





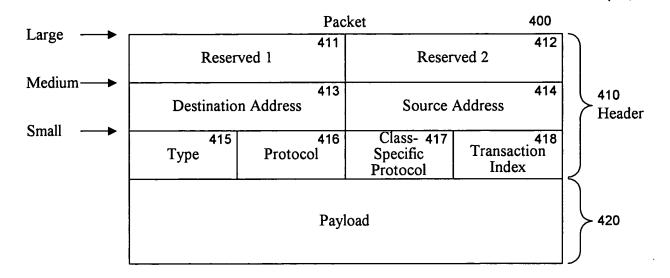
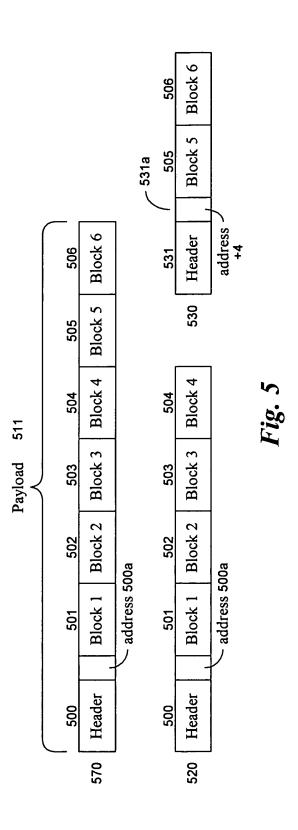


Fig. 4



The state of the s

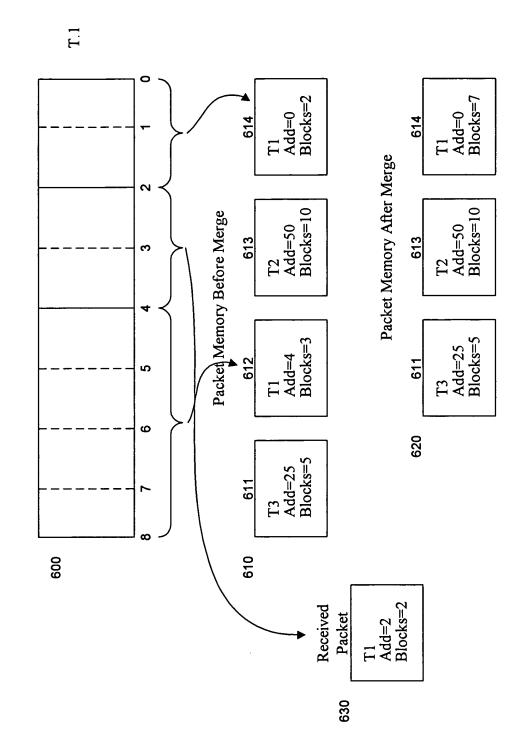


Fig. 6

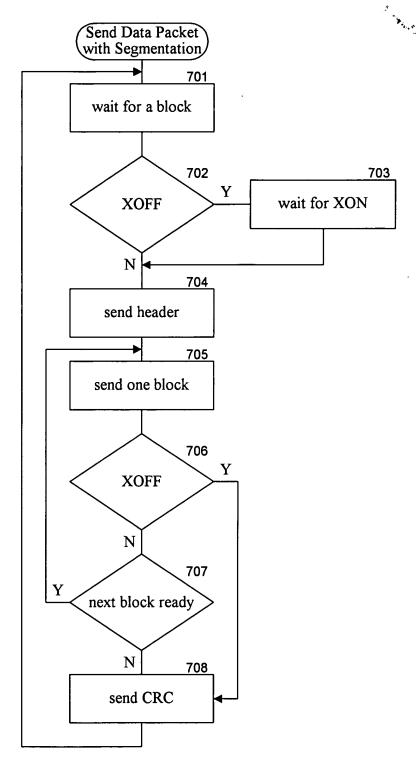


Fig. 7

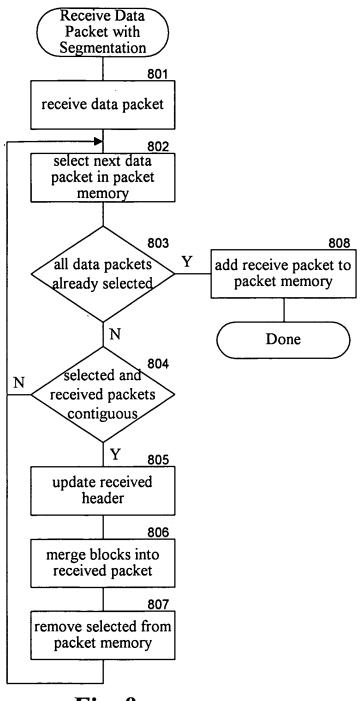
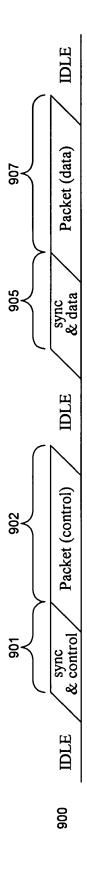


Fig. 8



sync & packet type

Fig. 9A

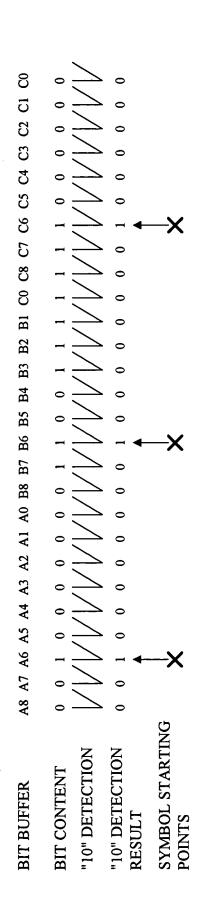


Fig. 9B

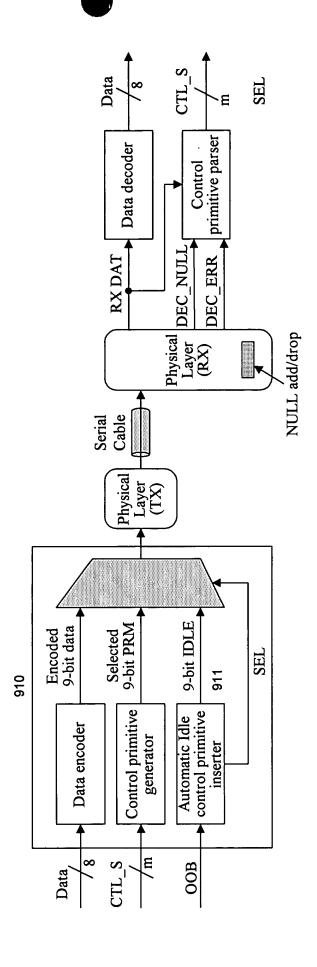


Fig. 9C

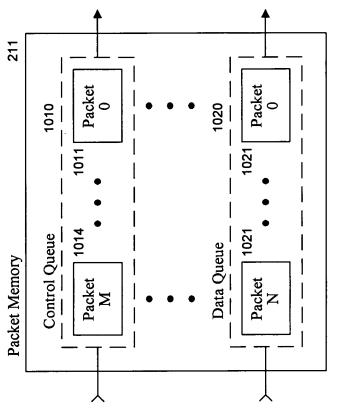


Fig. 10

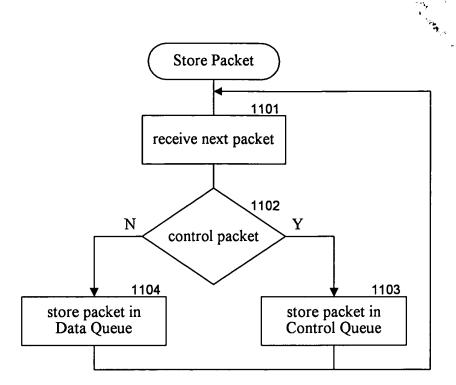


Fig. 11

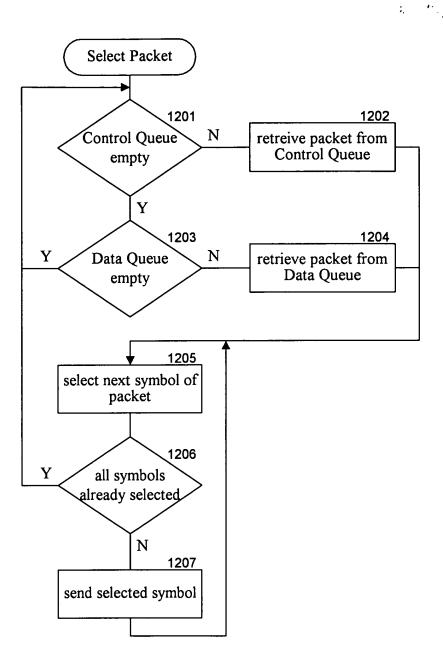


Fig. 12

IDLE data packet (cont'd) 1305 continue 1304 1303 control packet Preempt 1302 data packet 1301 DLE 1300

: <

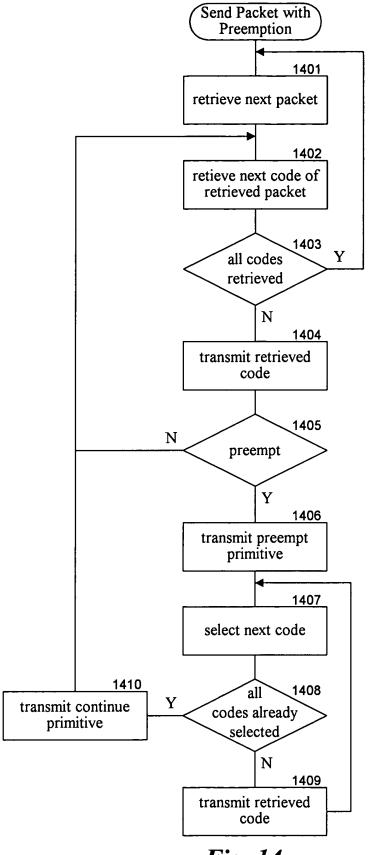


Fig. 14

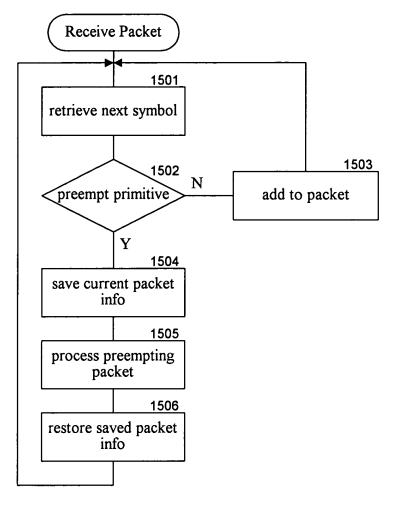


Fig. 15

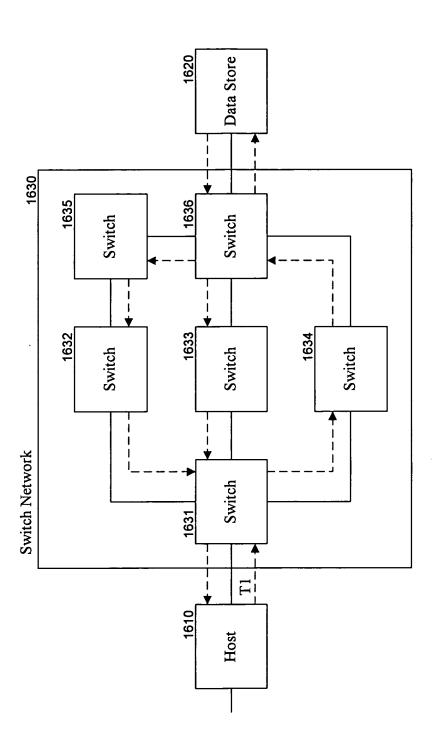


Fig. 10

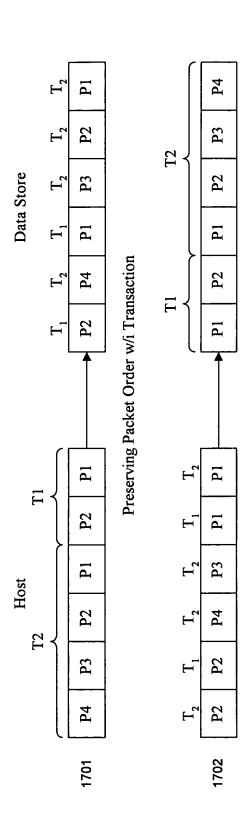


Fig. 17

No Packet or Transaction Ordering

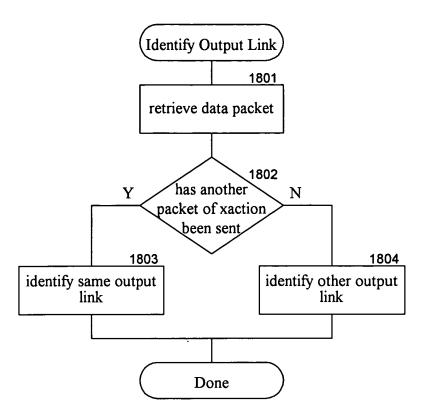


Fig. 18

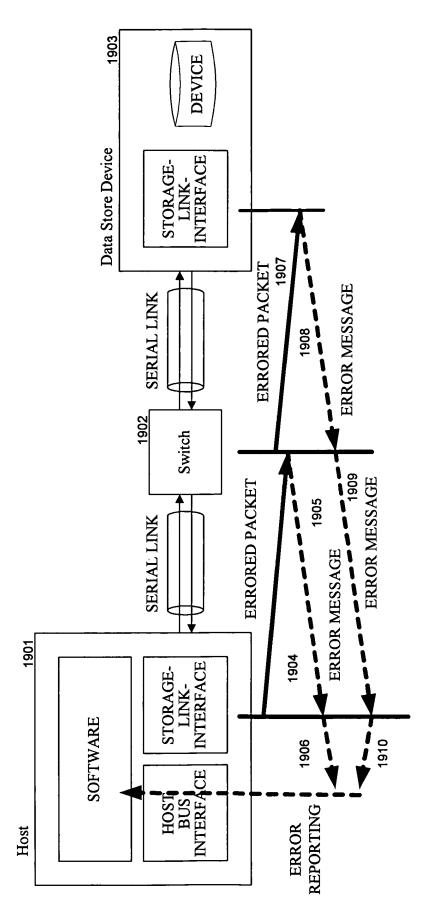


Fig. 19A

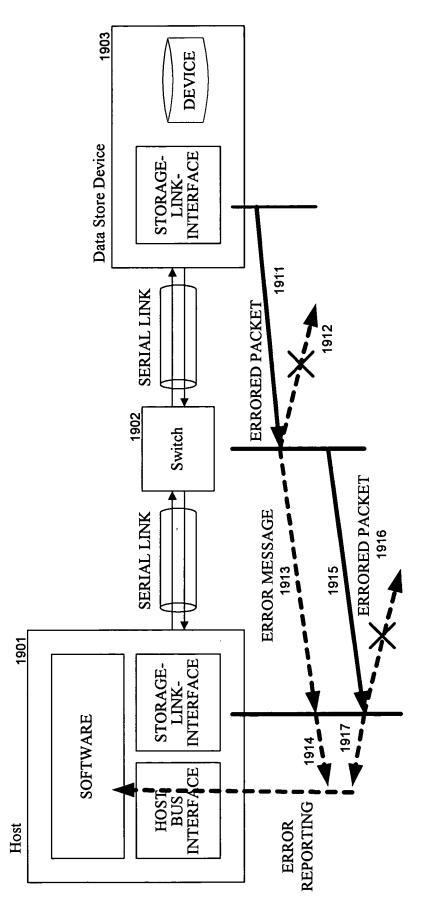


Fig. 19B

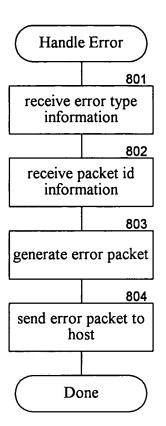


Fig. 19C

8b code		9 bit symbol
0000	0000	101010101
0000	0001	101010100
0000	0010	101010111
0101	0101	001010101
•		
0111	0110	001110110
0111	0 1 1 1	100100010
1111	1111	110101010

Fig. 20

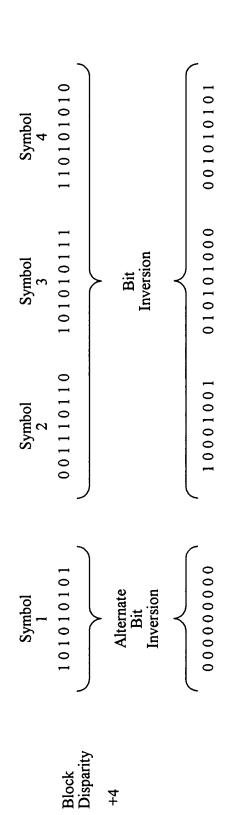
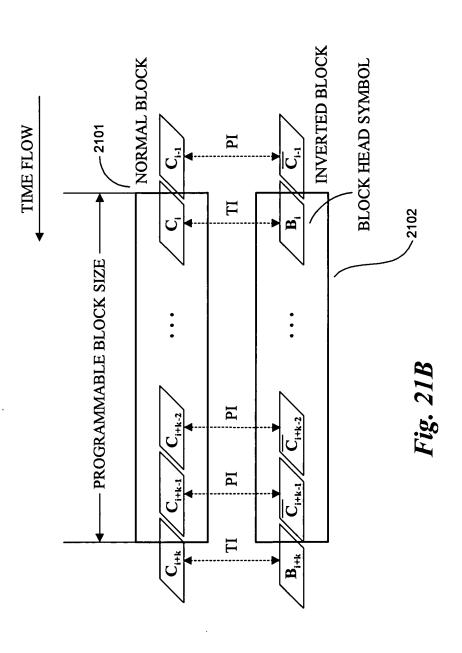


Fig. 21A



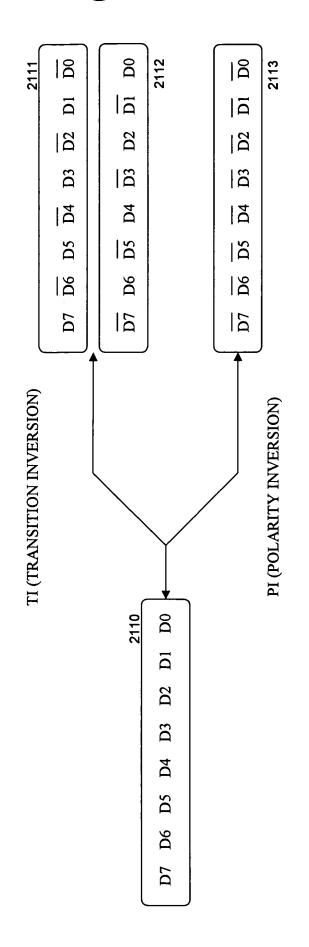


Fig. 21C

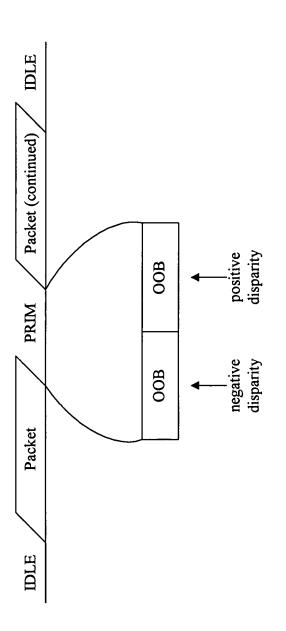


Fig. 22

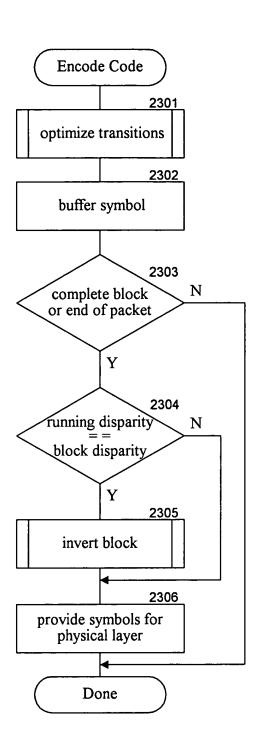


Fig. 23

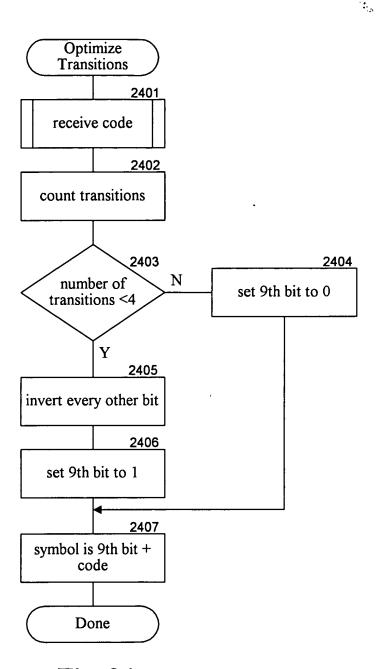


Fig. 24

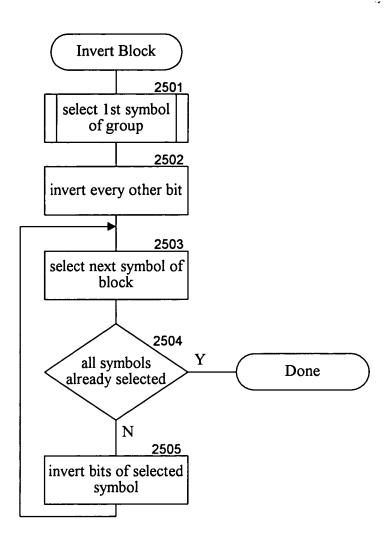
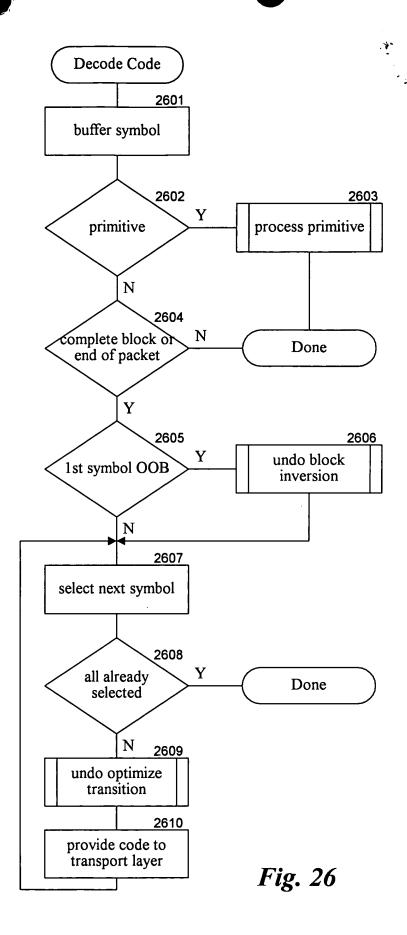


Fig. 25



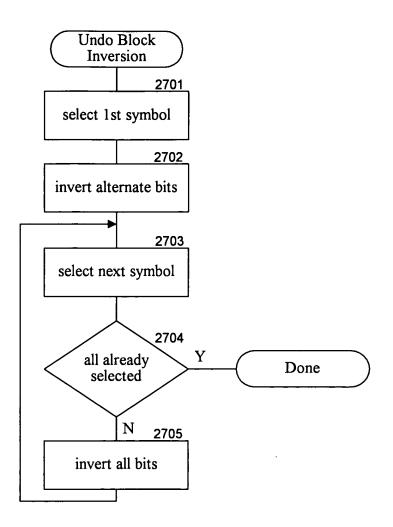


Fig. 27

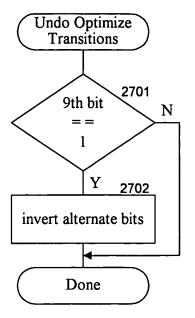


Fig. 28

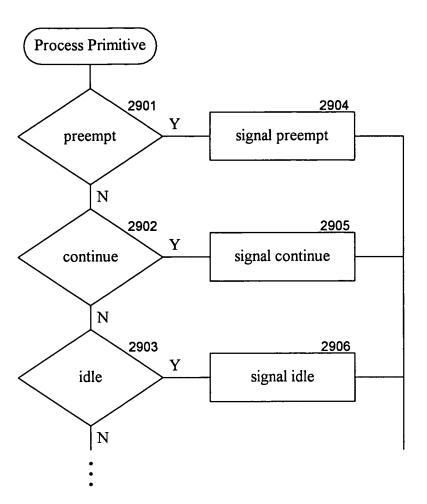
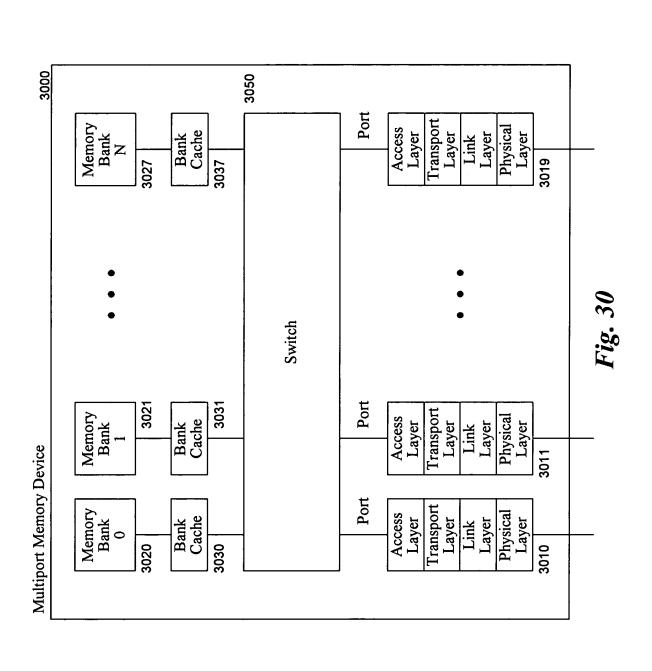


Fig. 29



4.

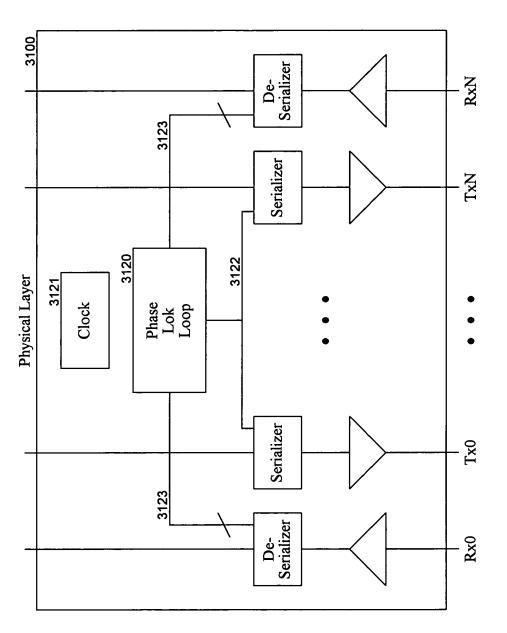


Fig. 31

Output Queue 3202	Valid Port Data	1 3 110	0	0	1 3 1011	•••
	>	:				
10						
3201	Data		101	1110		
Input Queue	R/W Address	1000	4000	1000	2000	
	R/W	R	M	W	R	• • •
	Port	3	4	3	3	

Fig. 32

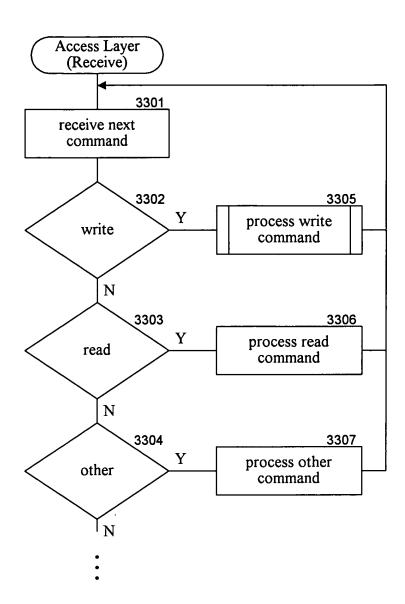


Fig. 33

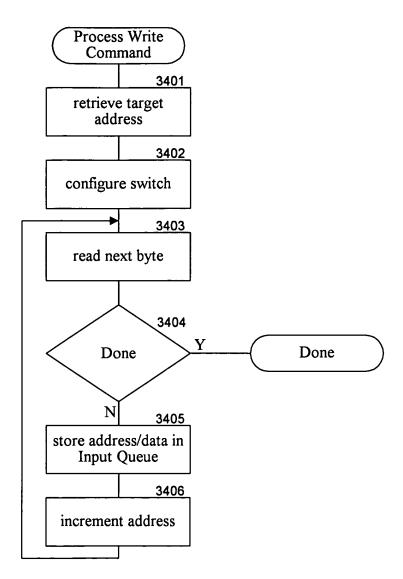


Fig. 34

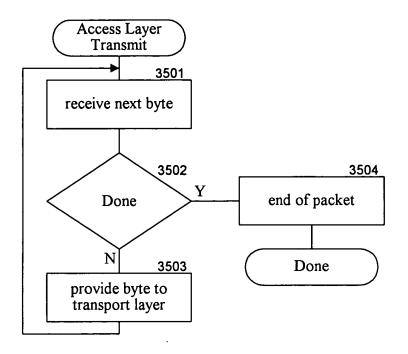
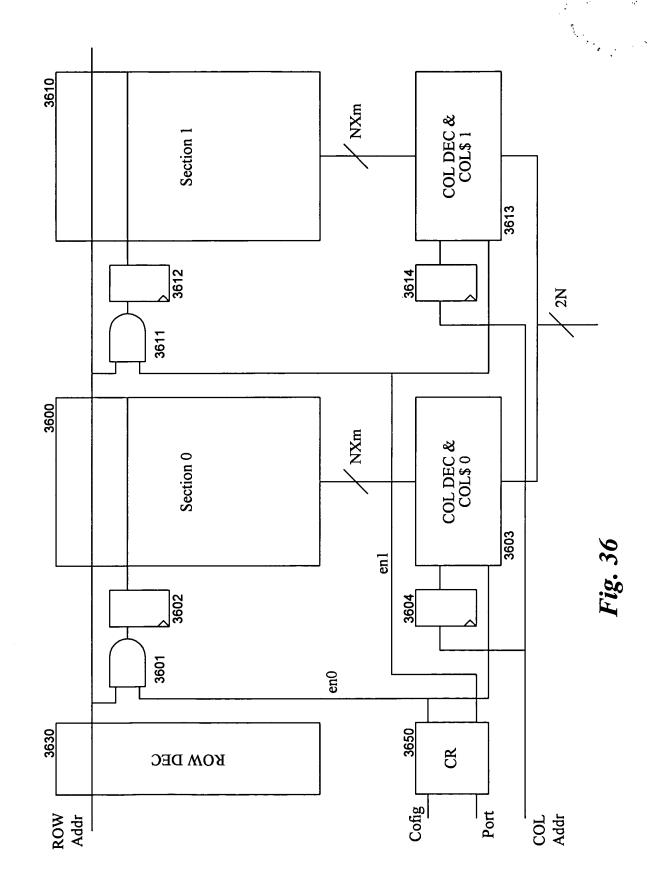


Fig. 35



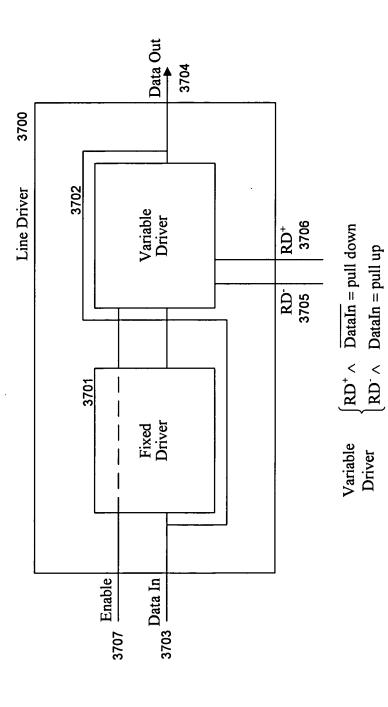


Fig. 37A

Tity :

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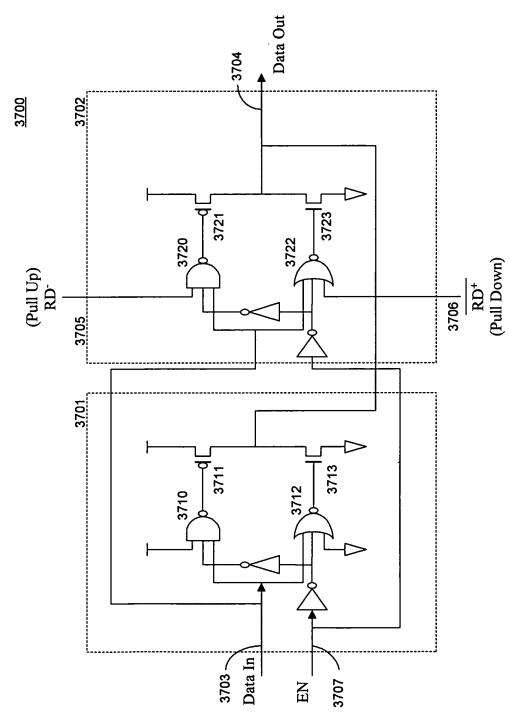


Fig. 37B

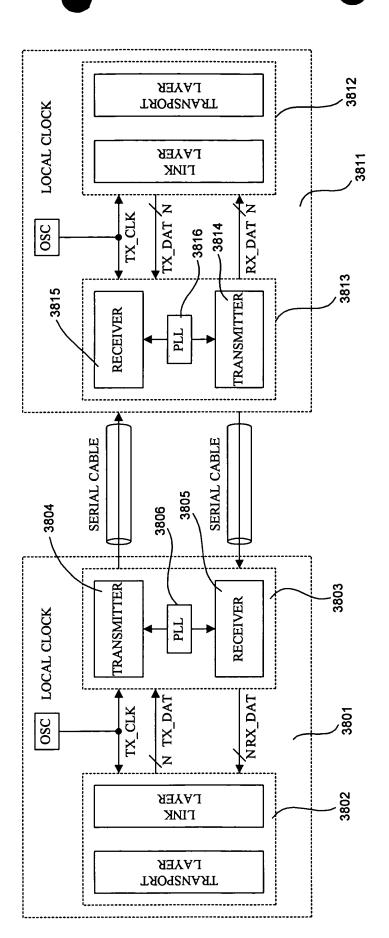


Fig. 38A

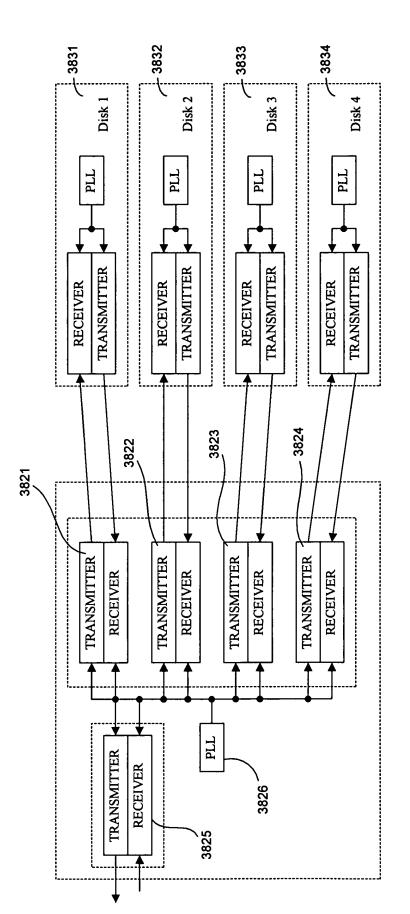
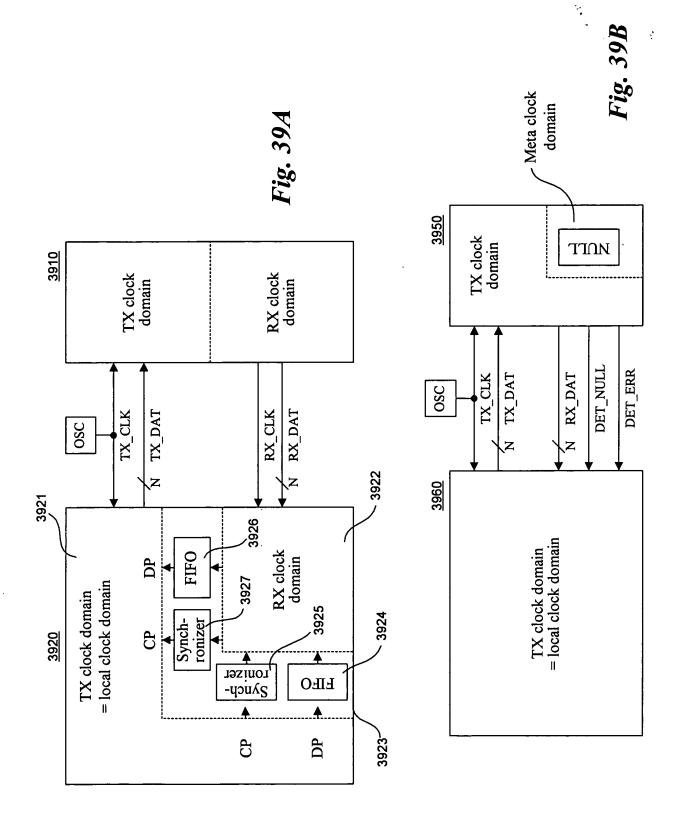
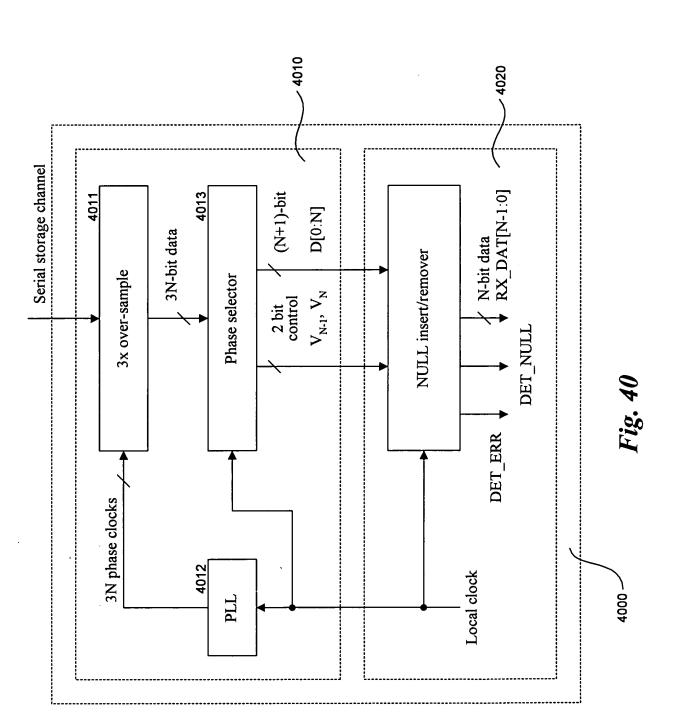
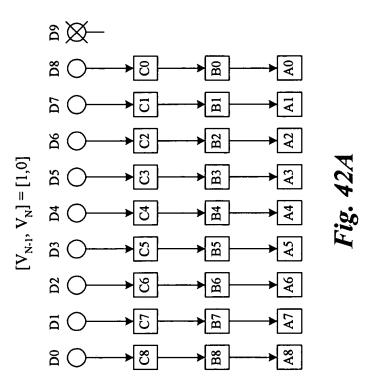


Fig. 38B







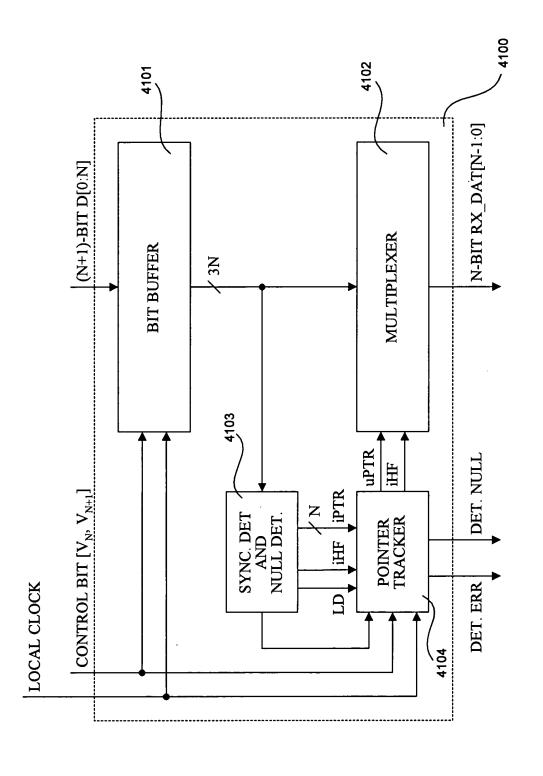


Fig. 4

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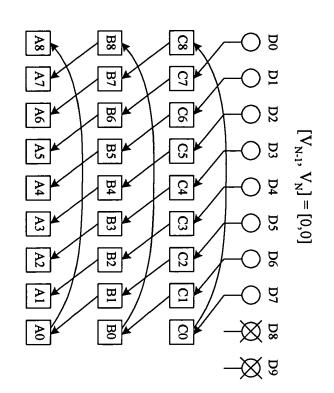


Fig. 42B

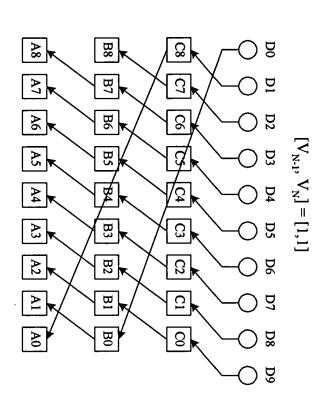


Fig. 42C

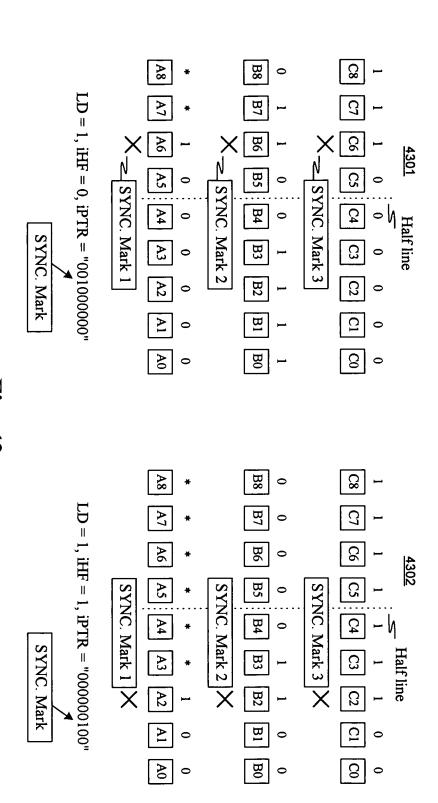


Fig. 43

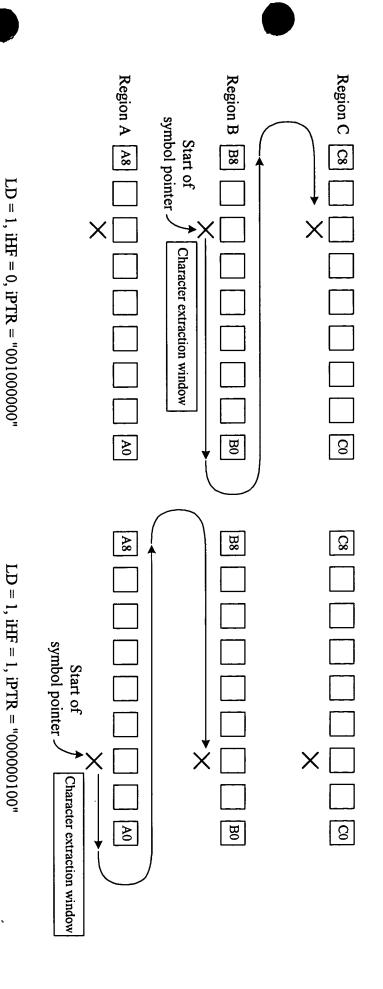
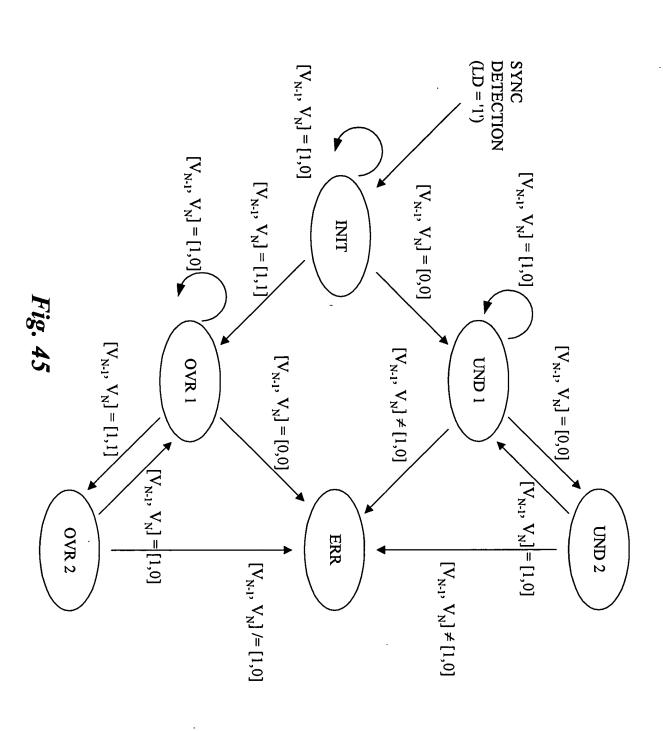


Fig. 44

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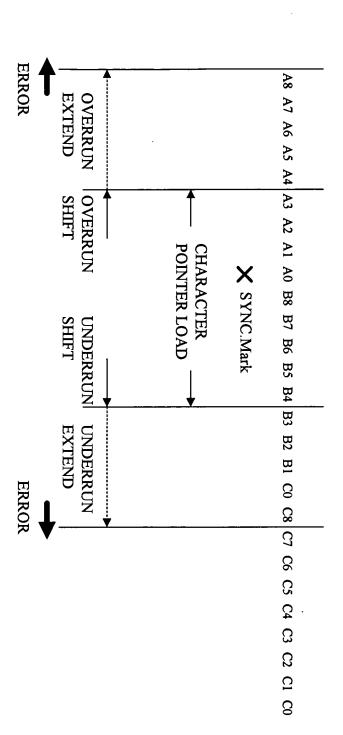


Fig. 46

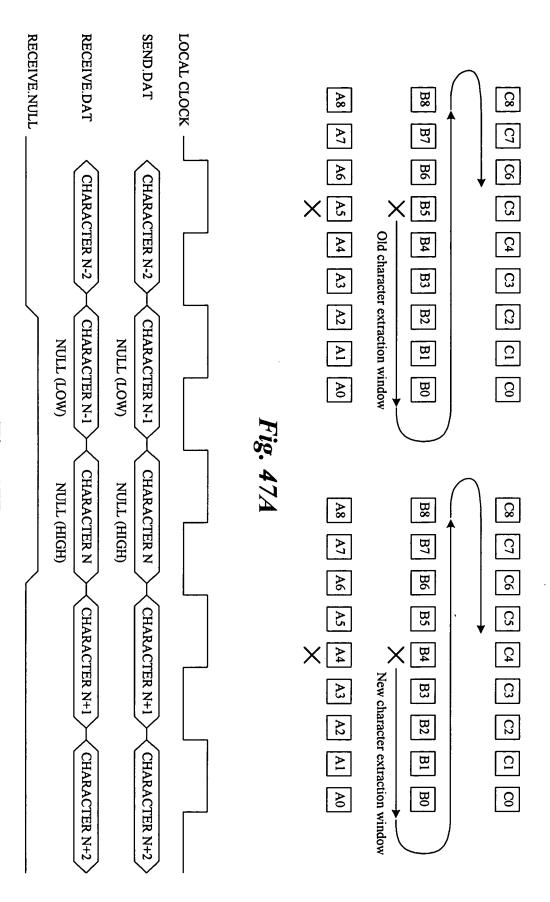


Fig. 47B

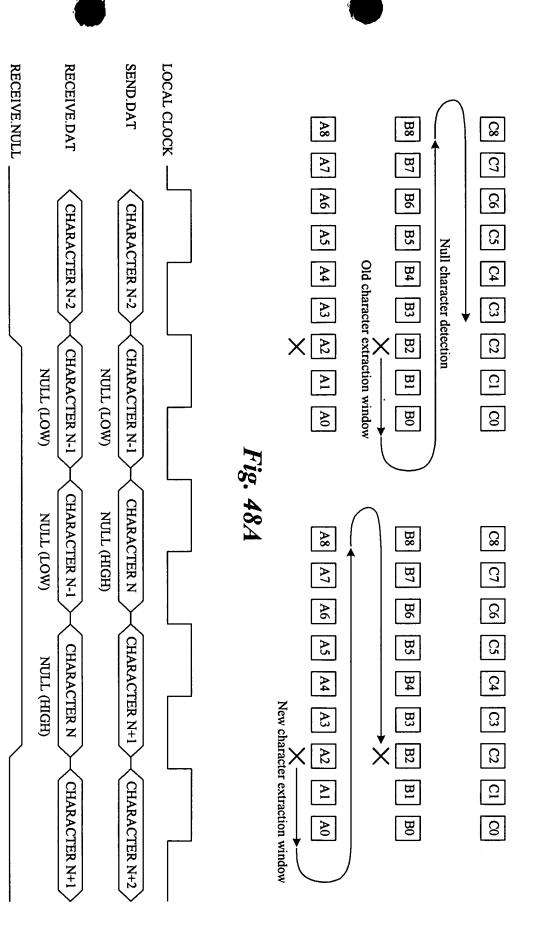


Fig. 48B

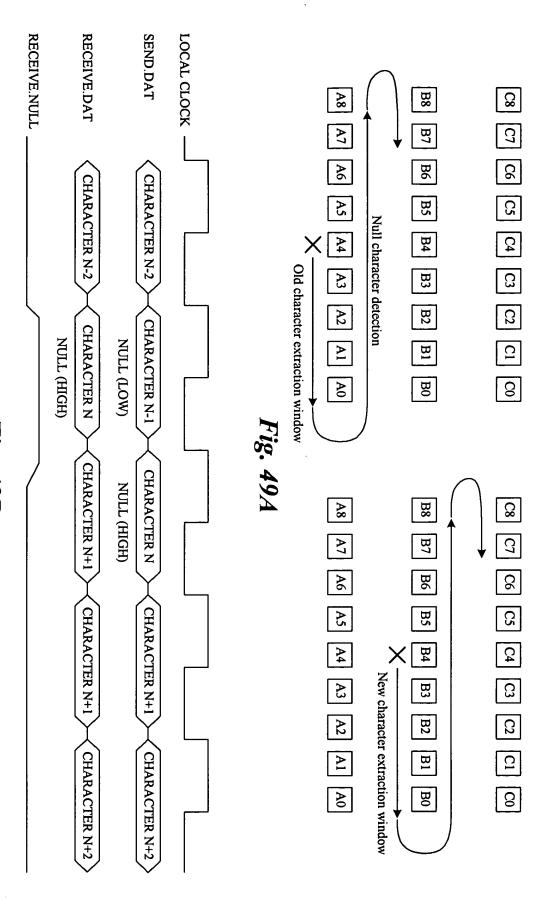


Fig. 49B